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survey and new results
Debardelaben, J.A.; Madisetti, V.K.;
Signals, Systems and Computers, 1995. 1995 Conference

the Twenty-Ninth Asilomar Conference on Volume 2, 30 Oct.-2 Nov. 1995 Page(s):1316 - 1320 Digital Object Identifier 10.1109/ACSSC.1995.540912

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P

3. Methodology for hardware/software co-verification Semeria, L.; Ghosh, A.; Design Automation Conference, 2000. Proceedings of 2000. Asia and South Pacific 25-28 Jan. 2000 Page(s):405 - 408 Digital Object Identifier 10.1109/ASPDAC.2000.83513

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4. Integrating assertion-based verification into syste

synthesis methodology Hessabi, S.; Gharehbaghi, A.M.; Yaran, B.H.; Goudar Microelectronics, 2004. ICM 2004 Proceedings. The 1

Conference on 6-8 Dec. 2004 Page(s):232 - 235

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5. Verification of transaction-level SystemC models (П testbenches Jindal, R.; Jain, K.; <u>Formal Methods and Models for Co-Design, 2003. ME</u> <u>Proceedings. First ACM and IEEE International Confe</u> 24-26 June 2003 Page(s):199 - 203 Abstract | Full Text: PDF(213 KB) IEEE CNF Rights and Permissions 6. Effective co-verification of IEEE 802.11a MAC/PHY П emulation and simulation technology II-Gu Lee; Seung-Beom Lee; Sin-Chong Park; Simulation Symposium, 2005. Proceedings. 38th Anni 4-6 April 2005 Page(s):138 - 146 Digital Object Identifier 10.1109/ANSS.2005.19 Abstract | Full Text: PDF(360 KB) IEEE CNF Rights and Permissions 7. Re-useable hardware/software co-verification of IF Bruce, A.; Goodenough, J.; ASIC/SOC Conference, 2001. Proceedings. 14th Ann International 12-15 Sept. 2001 Page(s):413 - 417 Digital Object Identifier 10.1109/ASIC.2001.954737 Abstract | Full Text: PDF(432 KB) IEEE CNF Rights and Permissions 8. Hardware/software co-design in the rapid prototyr. application-specific signal processors methodolog Schaming, W.B.;
VHDL International Users' Forum, 1997. Proceedings
19-22 Oct. 1997 Page(s):241 - 250 Digital Object Identifier 10.1109/VIUF.1997.623956 Abstract | Full Text: PDF(1164 KB) IEEE CNF Rights and Permissions 9. Virtual in-circuit emulation for timing accurate sys Benini, L.; Bruni, D.; Drago, N.; Fummi, F.; Poncino, N. ASIC/SOC Conference, 2002. 15th Annual IEEE Inter 25-28 Sept. 2002 Page(s):49 - 53 Abstract | Full Text: PDF(434 KB) IEEE CNF Rights and Permissions 10. Codesign of embedded systems based on Java a reconfigurable hardware components Fleischmann, J.; Buchenrieder, K.; Kress, R.; Design, Automation and Test in Europe Conference a 1999. Proceedings 9-12 March 1999 Page(s):768 - 769 Digital Object Identifier 10.1109/DATE.1999.761222 Abstract | Full Text: PDF(28 KB) IEEE CNF Rights and Permissions

11. Transaction level model-based design methodolo architectural exploration and verification

Cheng, W.; Wu, P.; Mastroleon, L.; Hakansson, M.; Circuits and Systems, 2003. MWSCAS '03. Proceedil IEEE International Midwest Symposium on Volume 3, 27-30 Dec. 2003 Page(s):1371 - 1374 Vol Abstract | Full Text: PDF(2208 KB) IEEE CNF Rights and Permissions

- 12. A multi-level design flow for incorporating IP core
 1D wavelet IP integration
 Baganne, A.; Bennour, I.; Elmarzougui, M.; Gaiech, F
 Design, Automation and Test in Europe Conference a
 2003
 2003 Page(s):250 255 suppl.
 Digital Object Identifier 10.1109/DATE.2003.1253837
 Abstract | Full Text: PDF(457 KB) IEEE CNF
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- 13. A debug sub-system for embedded-system co-ve Liu Jianhua; Zhu Ming; Bian Jinian; Xue Hongxi; ASIC, 2001. Proceedings. 4th International Conference 23-25 Oct. 2001 Page(s):777 780
 Digital Object Identifier 10.1109/ICASIC.2001.982678
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- 14. Automating formal modular verification of asynch time embedded systems
 Pao-Ann Hsiung; Shu-Yu Cheng;
 VLSI Design, 2003. Proceedings. 16th International C
 4-8 Jan. 2003 Page(s):249 254
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